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Bilbao

electrónica general

Lógica Combinacional

tema 6

DEPARTAMENTO DE TECNOLOGÍA ELECTRÓNICA

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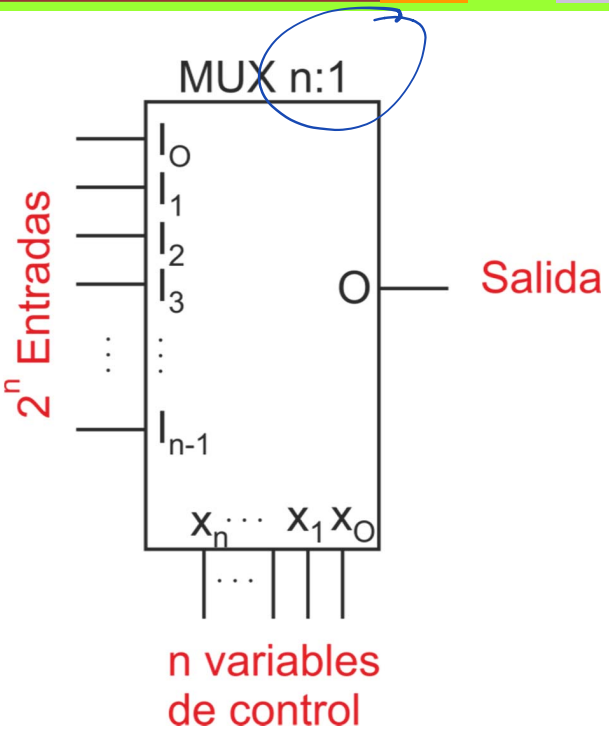
1.- Multiplexor

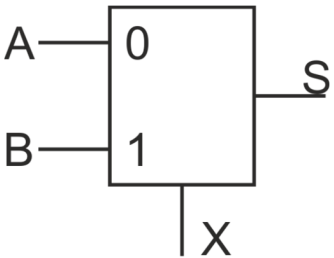
Circuito combinacional con:

- 2^n entradas,
- 1 salida
- n variables de control

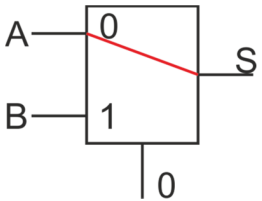


Con las variables de control seleccionamos cual de las entradas se conecta a la salida

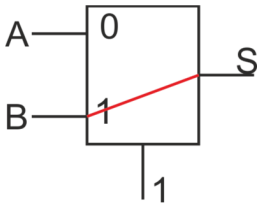
MUX 2:1



X = 0

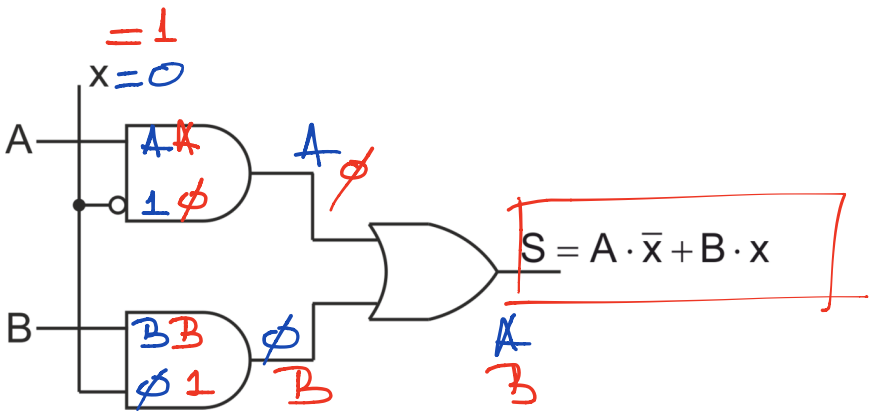


X = 1

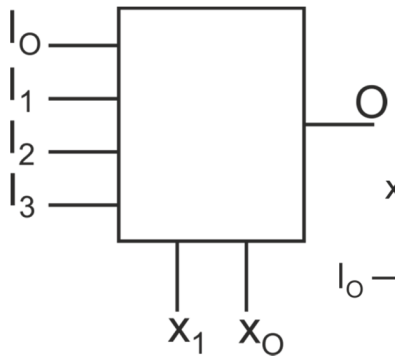


X	S
0	A
1	B

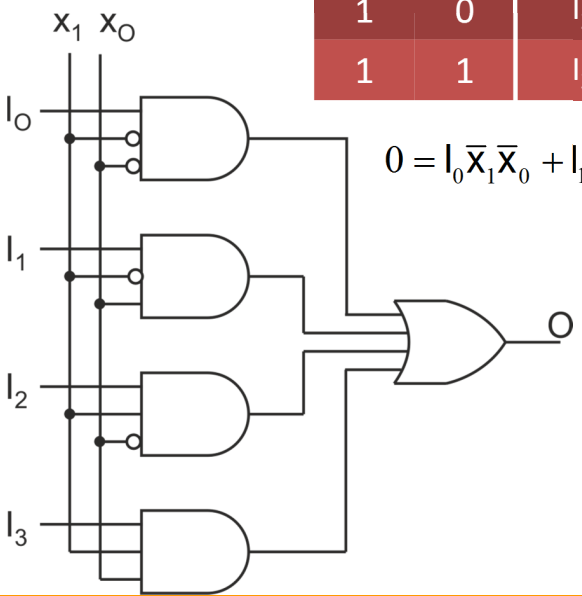
Con puertas lógicas



MUX 4:1

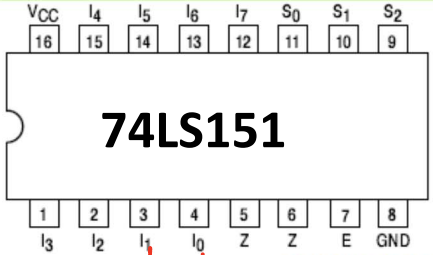


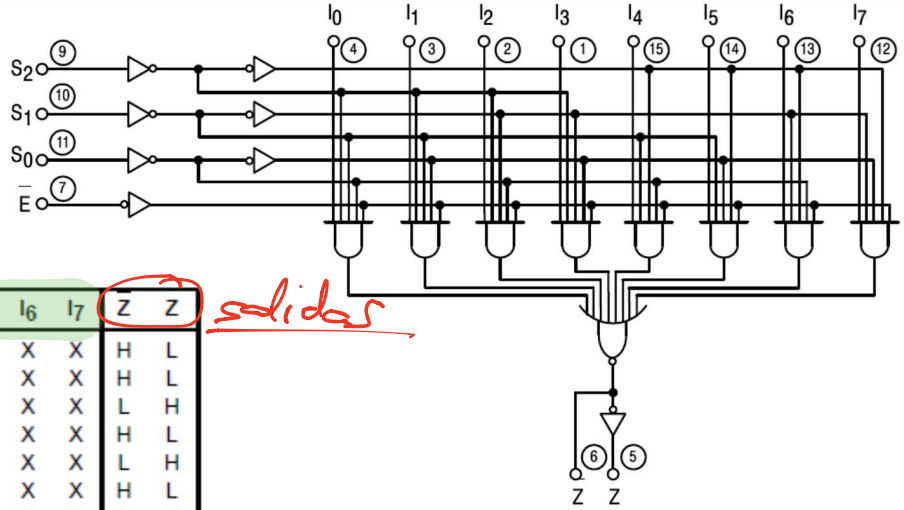
X_1	X_0	O
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



$$0 = I_0\overline{x}_1\overline{x}_0 + I_1\overline{x}_1x_0 + I_2x_1\overline{x}_0 + I_3x_1x_0$$

1.- Multiplexor





control

habilitador

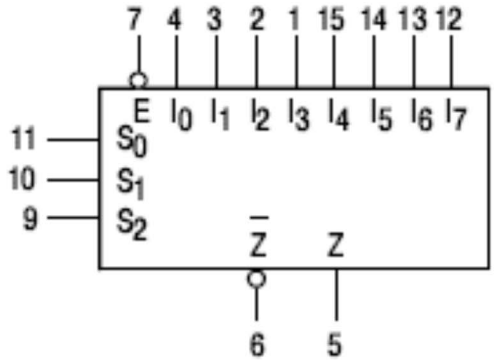
salidas

TRUTH TABLE

$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Z	$\overline{Z}$
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

E = Enable

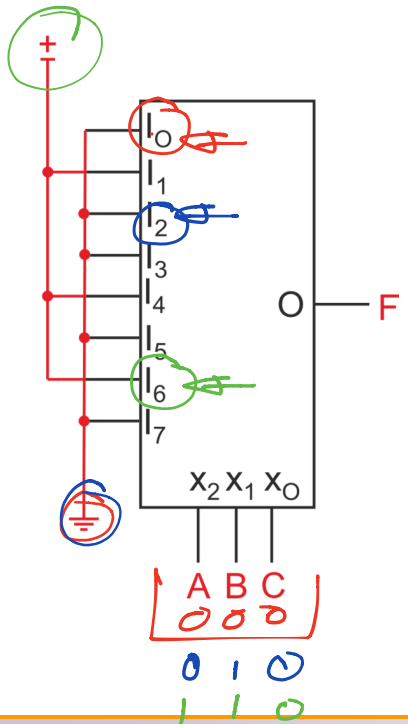


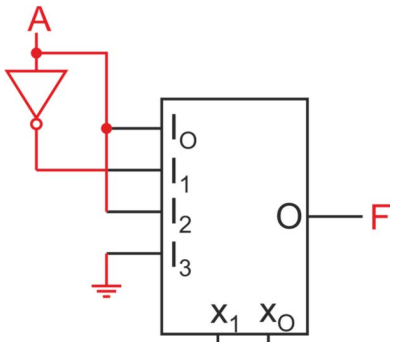
1.- Multiplexor

$$F = \bar{A}\bar{B}C + A\bar{B}\bar{C} + AB\bar{C}$$

Con un multiplexor de n señales de control se pueden hacer funciones de n+1 variables

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

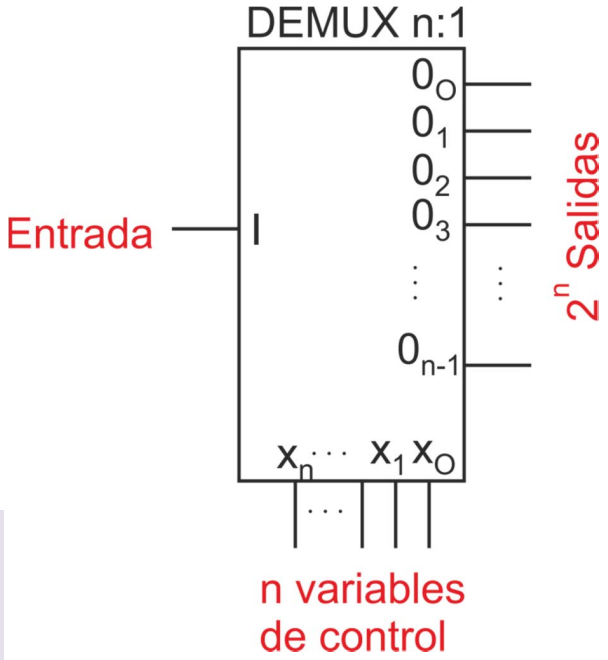




2.- Demultiplexor

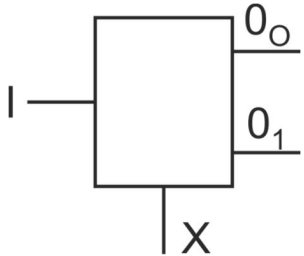
Circuito combinacional con:

- 1 entrada,
- 2^n salidas
- n variables de control

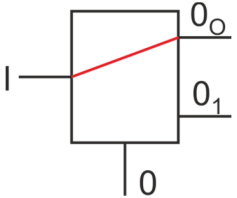


Con las variables de control seleccionamos cual de las salidas se conecta a la entrada

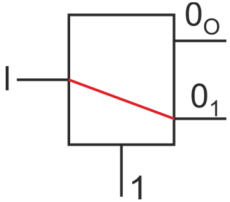
DEMUX 1:2



X = 0

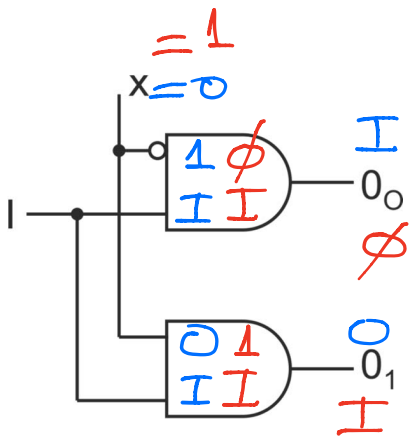


X = 1

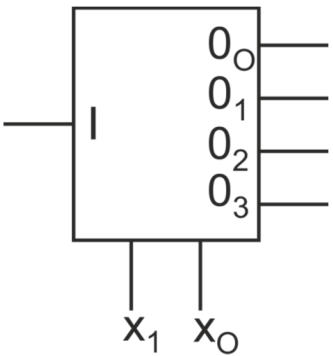


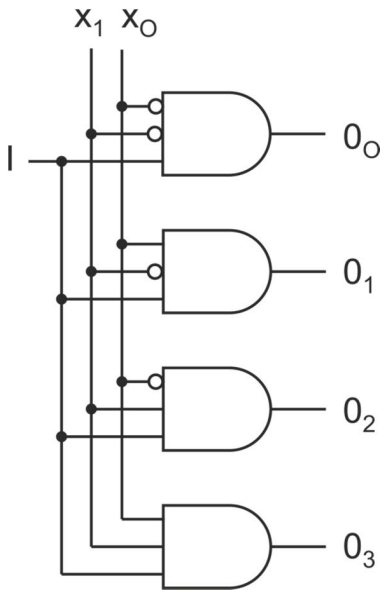
X	0_0	0_1
0	I	0
1	0	I

Con puertas lógicas



DEMUX 1:4





X_1	X_0	0_3	0_2	0_1	0_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

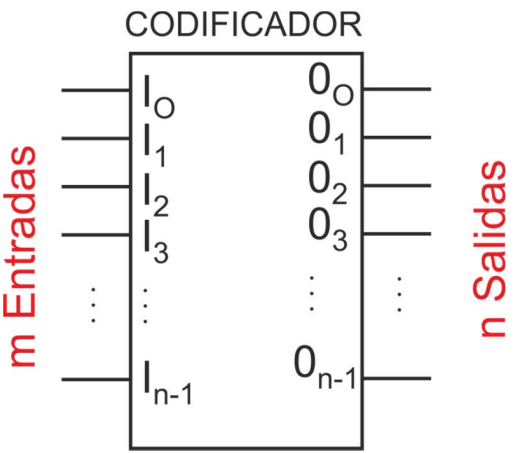
3.- Codificador

Circuito combinacional con:

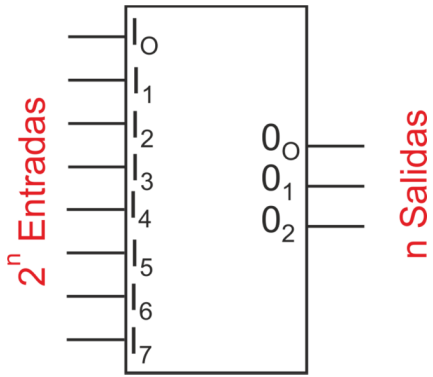
- m entradas
- n salidas

Si hay una entrada activa, a la salida aparece el código asignado a dicha entrada

Puede haber tantos tipos como códigos



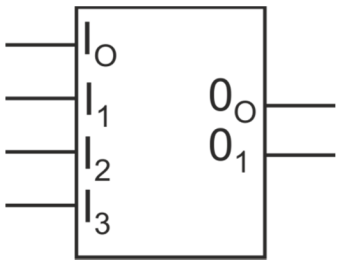
CODIFICADOR DECIMAL A BINARIO NATURAL



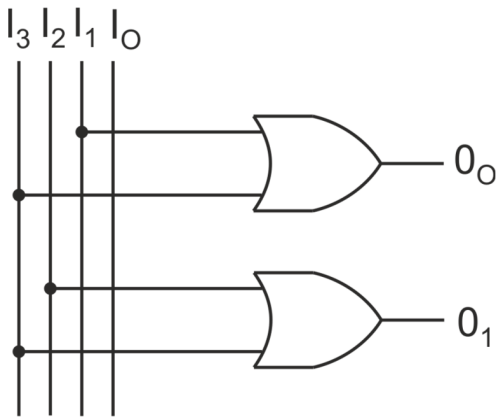
I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_2	O_1	O_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

¿Y si hay más de una entrada activa?

CODIFICADOR DECIMAL A BINARIO NATURAL



I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1



CODIFICADOR DE PRIORIDAD

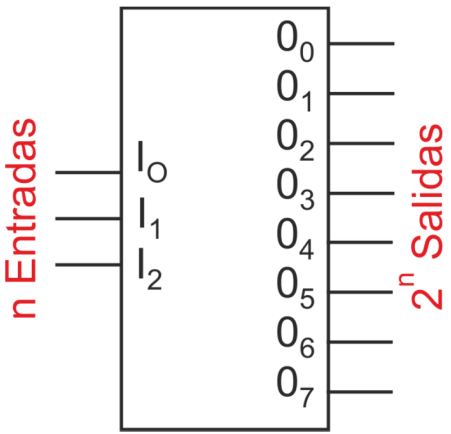
La salida responde a la entrada de mayor valor

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	X	0	0	1
0	0	0	0	0	1	X	X	0	1	0
0	0	0	0	1	X	X	X	0	1	1
0	0	0	1	X	X	X	X	1	0	0
0	0	1	X	X	X	X	X	1	0	1
0	1	X	X	X	X	X	X	1	1	0
1	X	X	X	X	X	X	X	1	1	1

4.- Decodificador

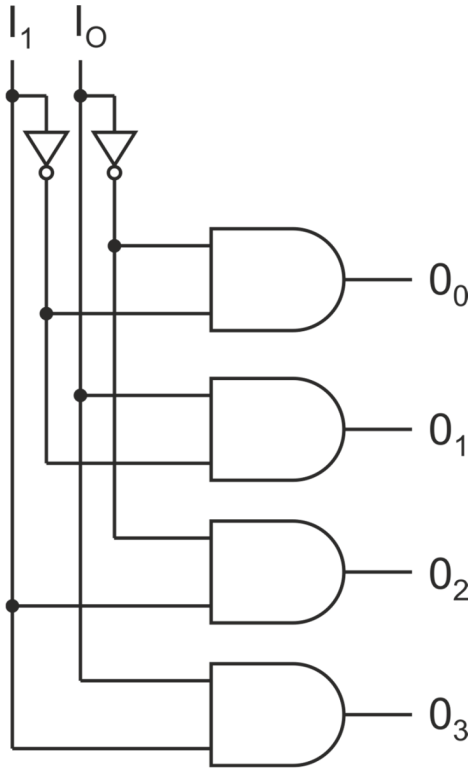
Realiza la operación inversa al codificador

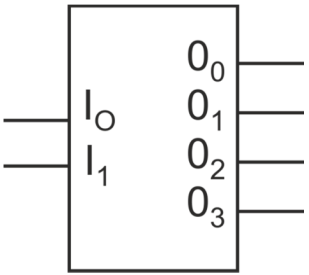
Para una combinación dada de n entradas activa una de sus 2^n salidas (para binario natural a decimal)



I_2	I_1	I_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	1	0	0	0	0	0	0	1	0	0
0	1	1	0	0	0	0	1	0	0	0
1	0	0	0	0	0	1	0	0	0	0
1	0	1	0	0	1	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0

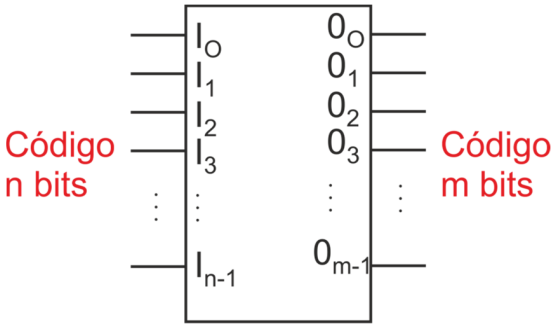
DECODIFICADOR BINARIO NATURAL A DECIMAL



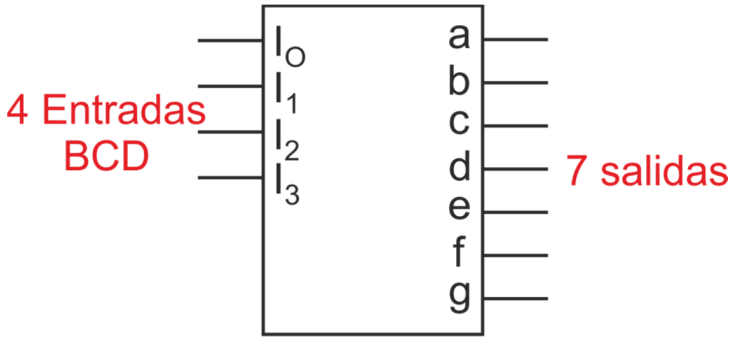


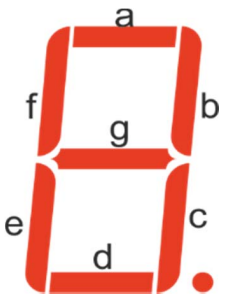
I_1	I_0	O_3	O_2	O_1	O_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

5.- Convertidor de código

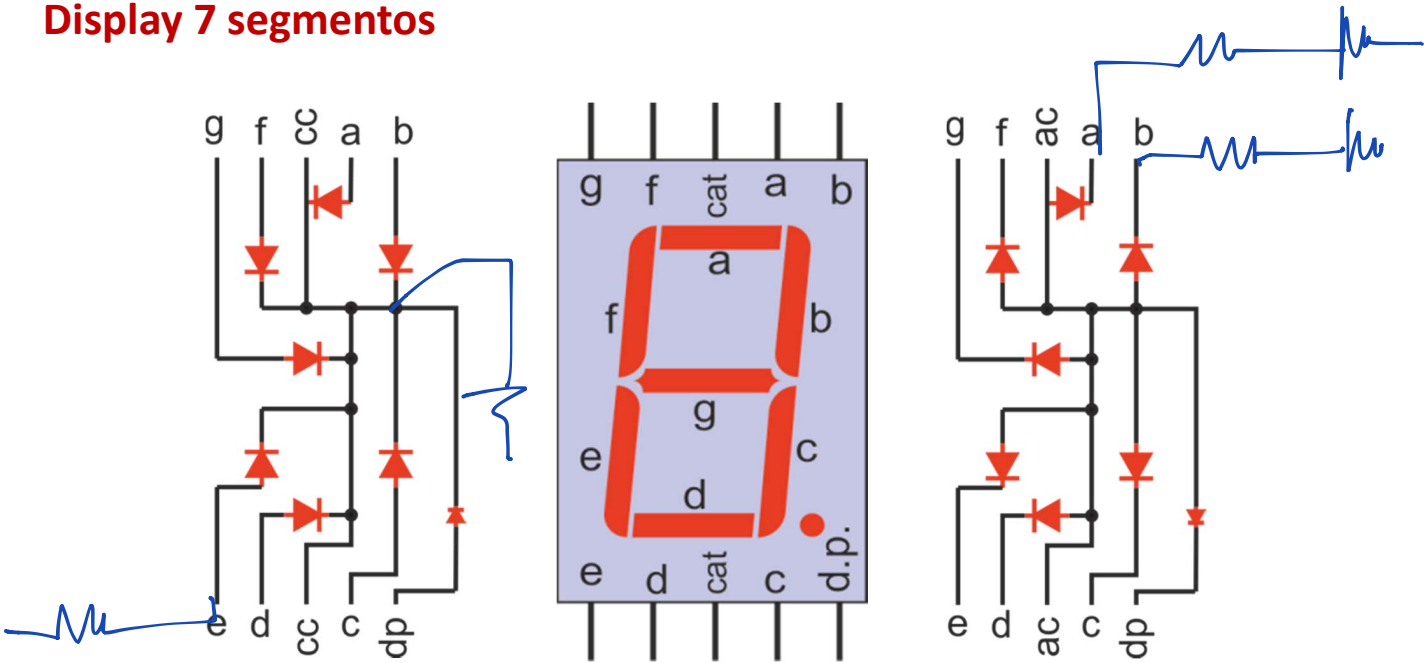


Uno muy habitual es el BCD/7 segmentos





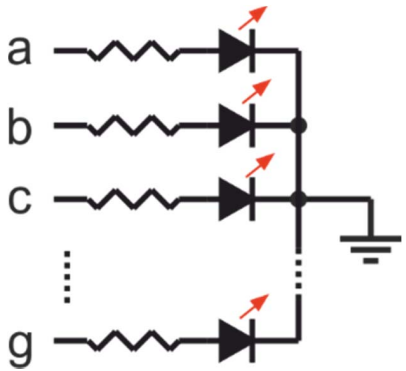
Display 7 segmentos



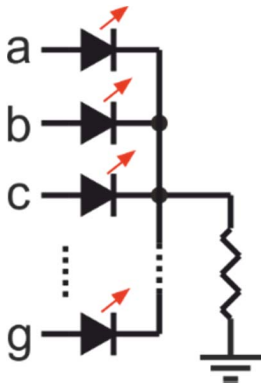
Cátodo Común **Ánodo Común**

Display 7 segmentos

Es imprescindible poner resistencias para limitar la corriente por los diodos



Todos los diodos lucen con igual intensidad siempre



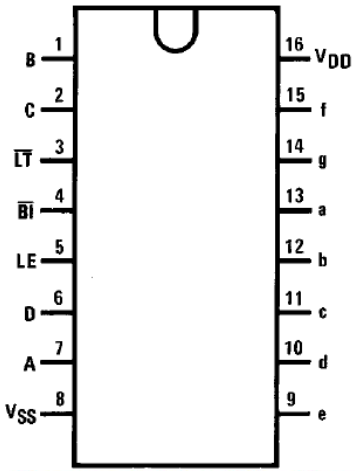
Los diodos lucen con distinta intensidad, dependiendo de cuantos estén en ON

5.- Convertidor de código

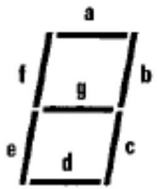
CD4511

Connection Diagram

Dual-In-Line Package



Segment Identification



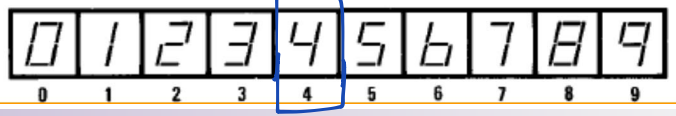
Truth Table

Inputs							Outputs							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	B
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				*

X = Don't Care

*Depends upon the BCD code applied during the 0 to 1 transition of LE.

Display



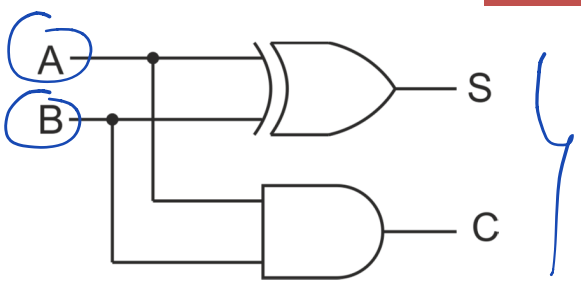
Semisumador

Circuito que realiza la suma de dos bits sin tener en cuenta la llevada

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$S = A \oplus B$

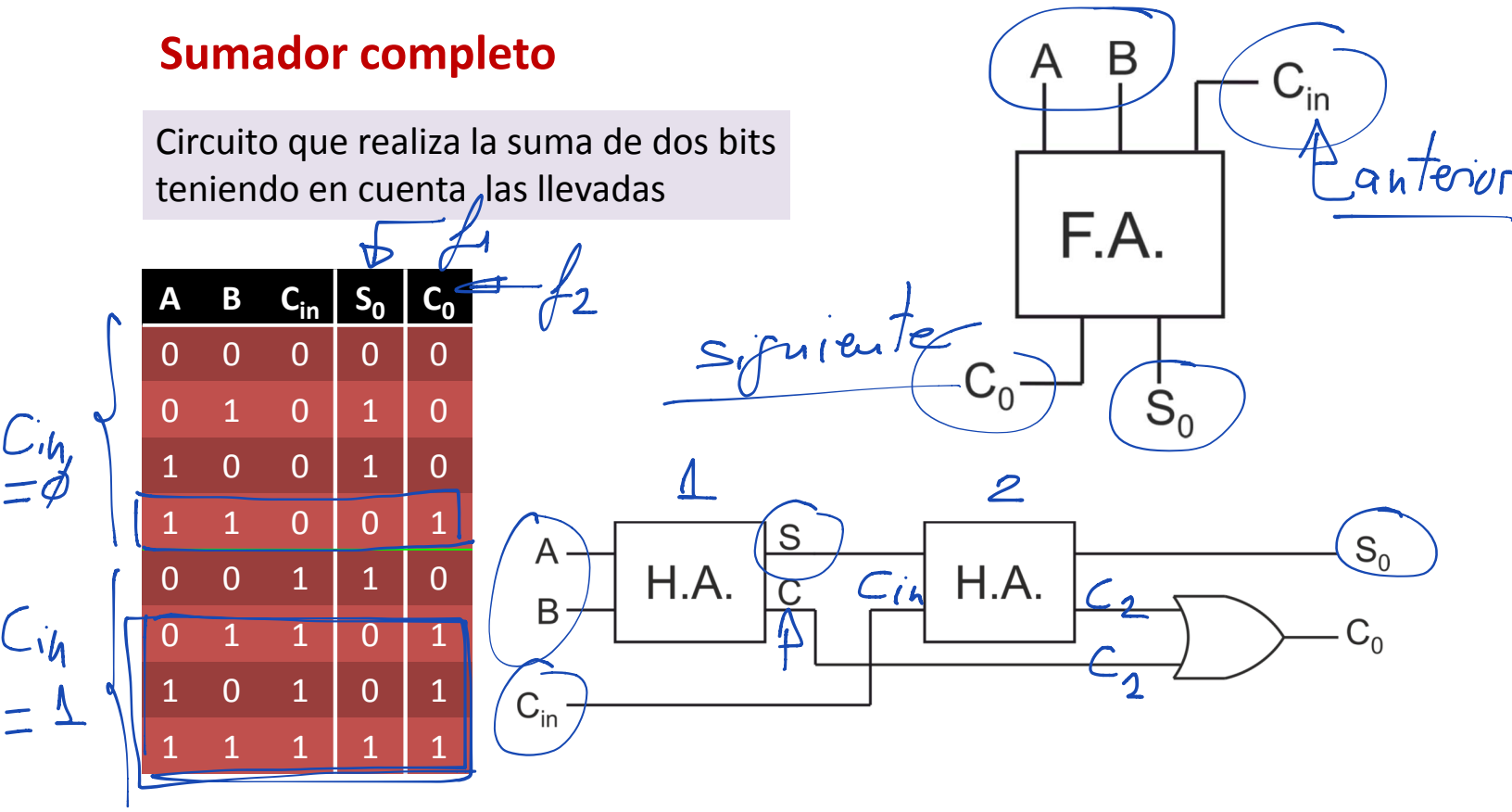
$C = A \cdot B$



Sumador completo

Circuito que realiza la suma de dos bits teniendo en cuenta las llevadas

A	B	C_{in}	S_0	C_0
0	0	0	0	0
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1
0	0	1	1	0
0	1	1	0	1
1	0	1	0	1
1	1	1	1	1



Sumador de 4 bits

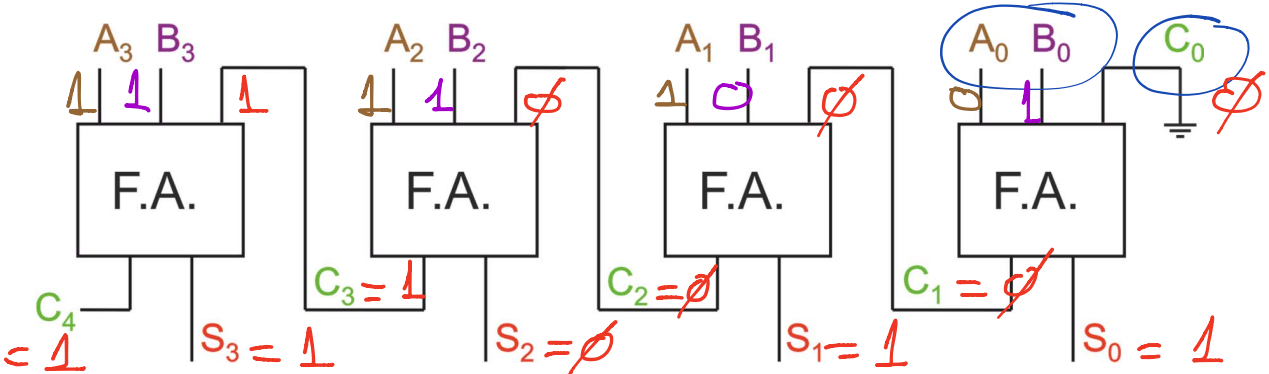
entero

$2^n = 27$

$n = \frac{\log 27}{\log 2}$

Full Adder

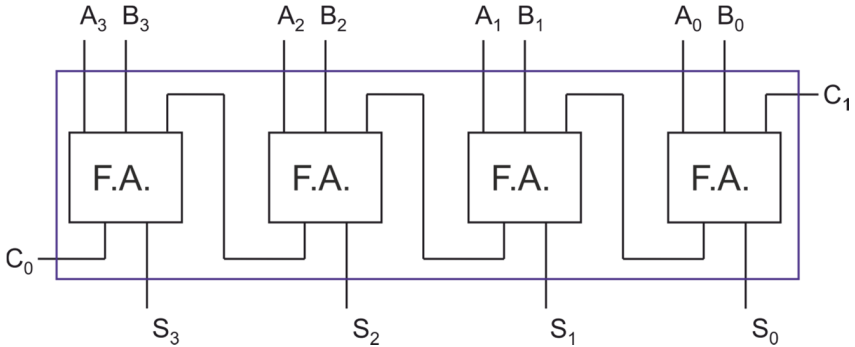
	C_3	C_2	C_1	C_0	
A	1 (A_3)	1 (A_2)	1 (A_1)	0 (A_0)	14
+ B	1 (B_3)	1 (B_2)	0 (B_1)	1 (B_0)	13
	C_4 = 1	S_3 = 1	S_2 = 0	S_1 = 1	S_0 = 1	27

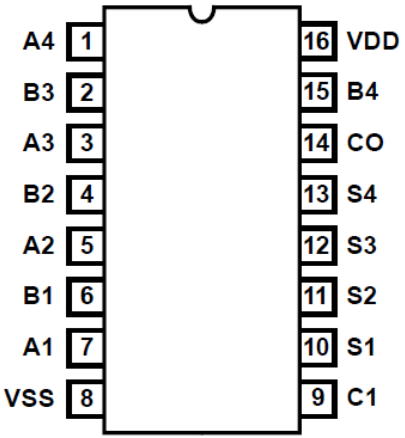


C = 1 1 0 1 1

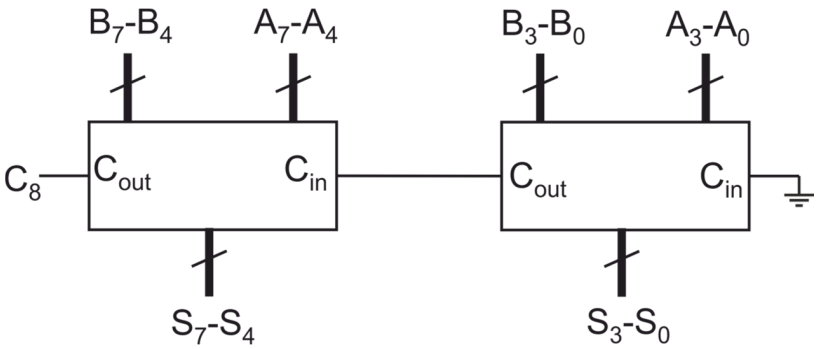
Sumador de 4 bits

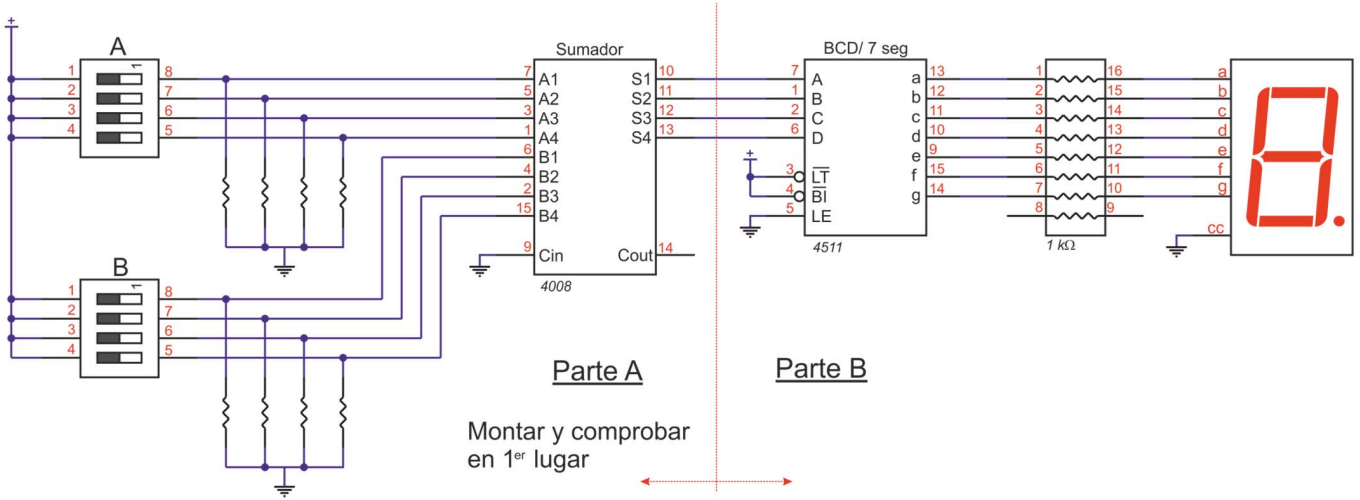
CD4008





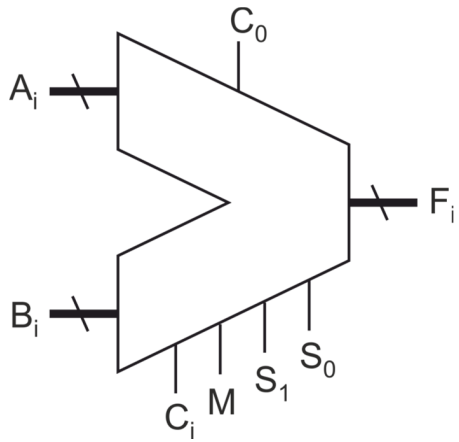
Se pueden acoplar en cascada para sumar números de más bits

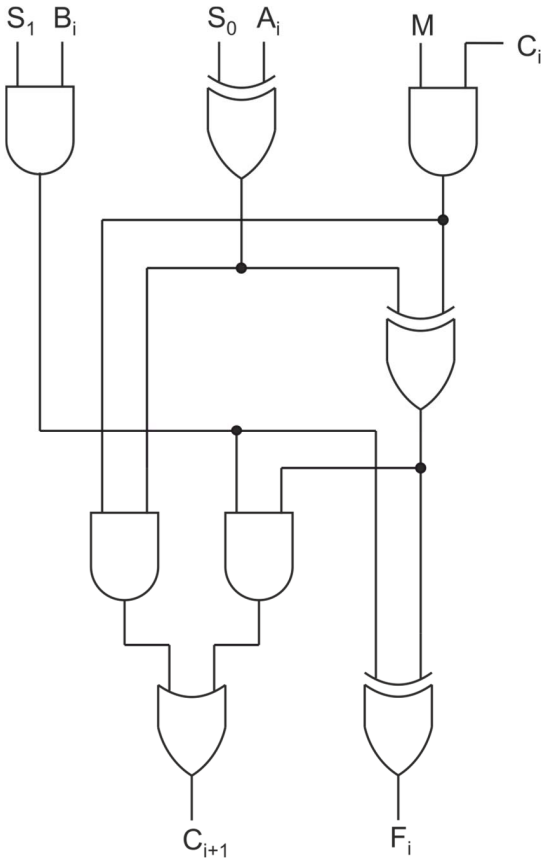



A
B
Sumador
A1
A2
A3
A4
B1
B2
B3
B4
Cin
S1
S2
S3
S4
Cout
4008
BCD/ 7 seg
A
B
C
D
LT
BI
LE
a
b
c
d
e
f
g
4511
1 kΩ
cc
Parte A
Parte B
Montar y comprobar
en 1er lugar

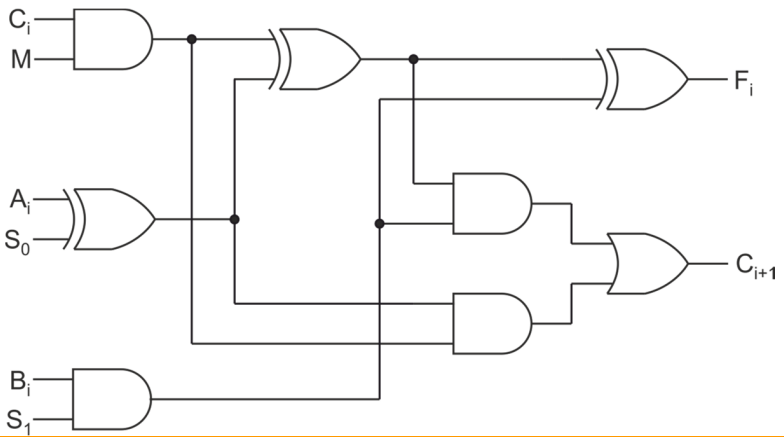
Arithmetic Logic Unit

Circuito combinacional que realiza operaciones aritméticas y/o lógicas dependiendo de unas variables de control

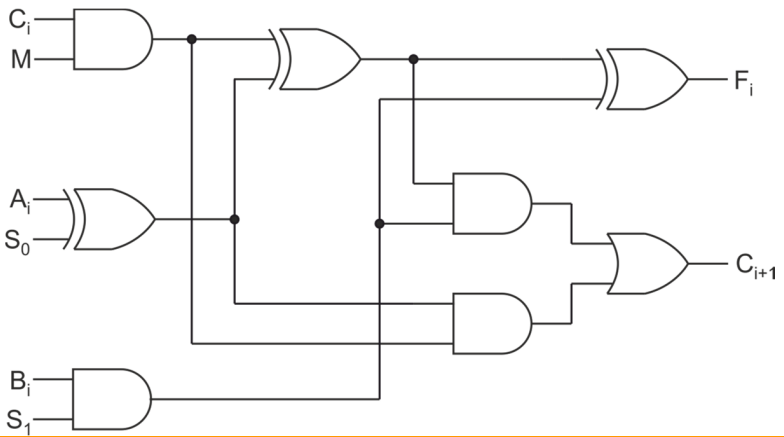




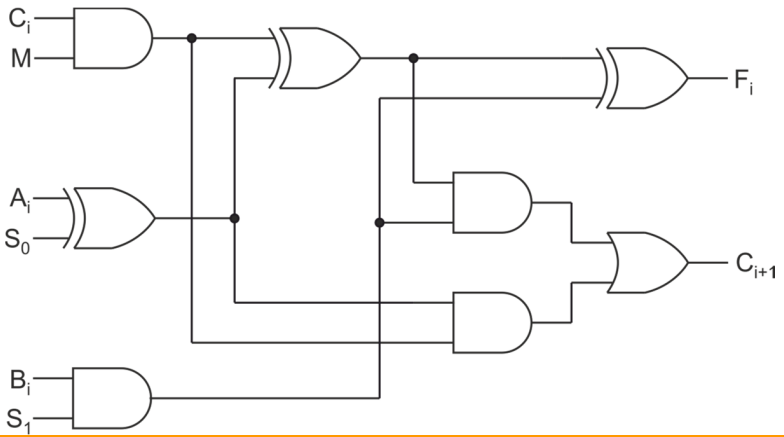
M=0 (Función Lógica)			
S_1	S_0	F_i (F. Lógica)	*Comentario*
0	0	$F_i = A_i$	Entrada ***A*** transferida a la salida
0	1	$F_i = \overline{A}_i$	Entrada ***A*** complementada y transferida
1	0	$F_i = A_i \oplus B_i$	XOR
1	1	$F_i = \overline{A_i \oplus B_i}$	XNOR



M=1 (Función Aritmética) y $C_i = 0$			
S_1	S_0	F_i (F. aritmética)	*Comentario*
0	0	$F_i = A_i$	Entrada ***A*** transferida a la salida
0	1	$F_i = \overline{A}_i$	Complemento a uno de *A*
1	0	$F_i = A_i + B_i$	Suma de ***A*** y ***B***
1	1	$F_i = \overline{A_i} + B_i$	Suma de ***B*** y el complemento a uno de ***A***



M=1 (Función Aritmética) y $C_i = 1$			
S_1	S_0	F_i (F. aritmética)	*Comentario*
0	0	$F_i = A_i + 1$	Incrementa ***A***
0	1	$F_i = \overline{A}_i + 1$	Complemento a dos de *A*
1	0	$F_i = A_i + B_i + 1$	Incrementa la suma de ***A*** y ***B***
1	1	$F_i = \overline{A_i} + B_i + 1$	***B*** menos ***A***



1 ← Llevada

3	0 1 1	(carry)
+ 2	0 1 0	
5	1 0 1	

$2^2\ 2^1\ 2^0$

$4 + 0 + 1 = 5$

1 más 1 = 2

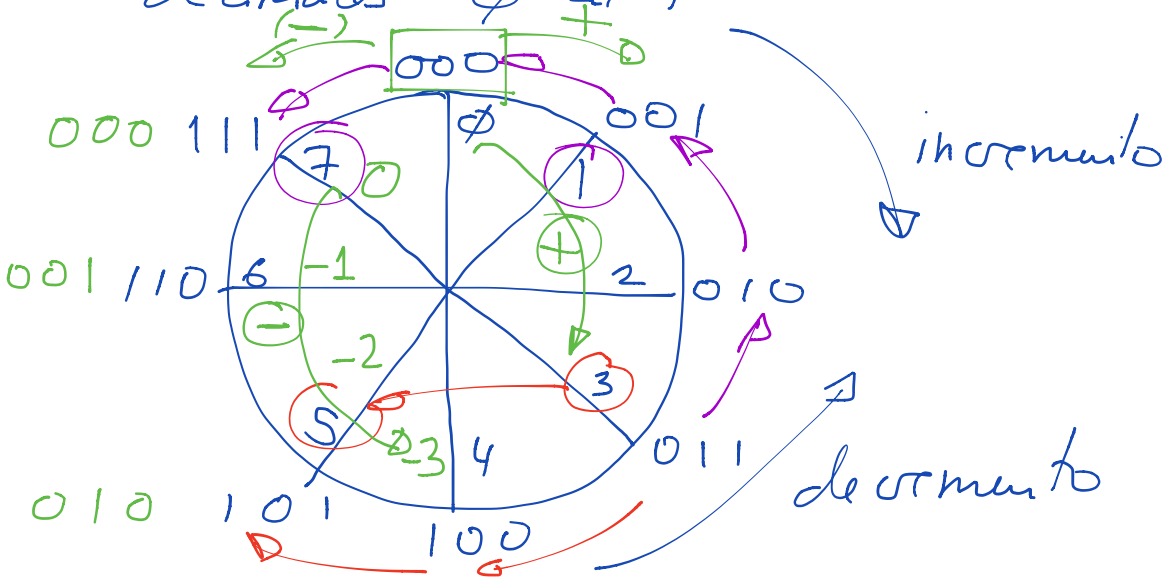
≠

1 OR 1 = 1

Complemento a 2

3 bits para representar un número

Puedo representar los números decimales ∅ al 7



3 + 2 = 5

3 − 2 = 1

3 − 4 = −1 ¿7?

complemento a 1

qué le falta a un número para llegar a 1

↳ es hallar la negada

1 1 1 ←

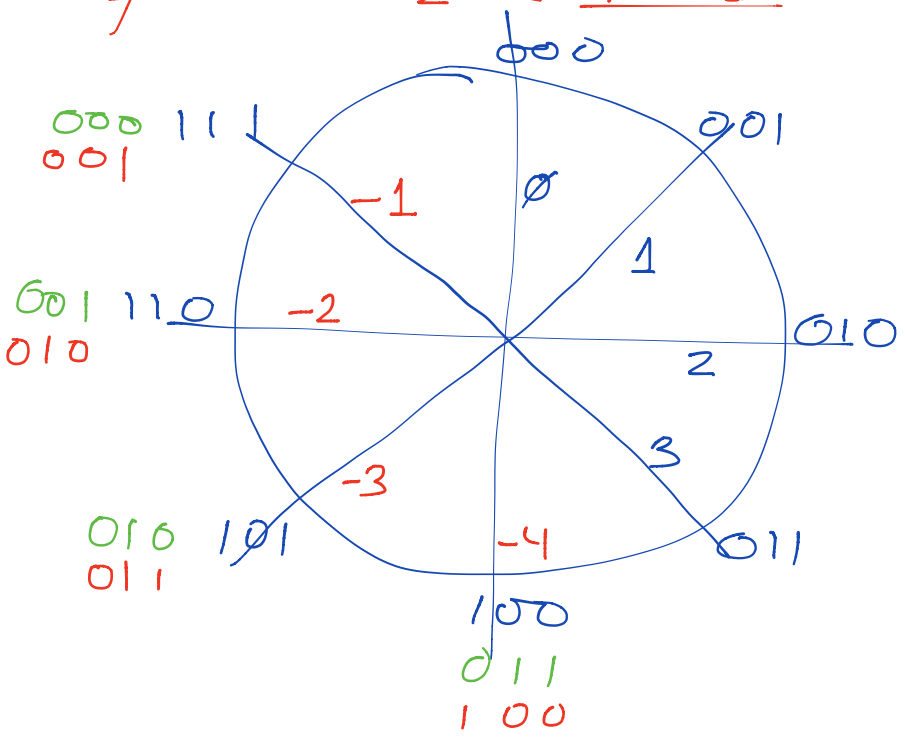
0 0 0 ← complemento a 1

1 0 1

0 1 0 ← complemento a 1

Con el complemento a 1 hay 2 ceros

Complemento a 2 es ~~A~~ + 1



$$\begin{array}{r} 3 \\ -4 \\ \hline -1 \end{array}$$

Sumamos a 3 el complemento a 2 de 4

nº 3 → 0 1 1

nº 4 → 1 0 0

↳ comp. a 1 → 0 1 1 + 1

↳ comp a 2 → 1 0 0 (−4)

$$\begin{array}{rr} 3 & 0\ 1\ 1 \\ +\ (-4) & 1\ 0\ 0 \\ \hline & \textcircled{1}\ 1\ 1 \leftarrow \end{array}$$

↑ es un nº negativo

↓ complemento a 2

1º → 0 0 0 (complemento a 1)

2º + 1

0 0 1 (complemento a 2)

↳ −1